IT IS CLAIMED:

1. A memory system, comprising:

a memory logically organized in M bit wide blocks as a plurality of rows of 2N columns, where N and M are positive integers; and

a memory interface, connected to the memory to receive an address specifying a memory block and supply the corresponding memory contents of up to (N+1) blocks, whereby said address is supplied to the first N of said columns, the memory interface comprising:

an adder connected to receive a first portion of the address and supply said first portion with one added one thereto, wherein said first portion of the address is sufficient to specify the row to which a block belongs; and

an input multiplex circuit connected to the second N of said columns to receive the address, the output of the adder, and a portion of the address sufficient to specify whether the address the specified block belongs to the first N of said columns, whereby the second N of said columns is supplied with the address when the specified block belongs to the second N of said columns and is supplied with the output of the adder when the specified block belongs to the first N of said columns.

2. The memory system of claim 1, the memory interface further comprising:

a memory disable circuit connected to receive a second portion of the address and disable (N-1) columns in response, wherein said second portion of the address is sufficient to specify the column to which a block belongs.

3. The memory system of claim 2, wherein the memory is an embedded memory of a microprocessor.

4. The memory system of claim 3, wherein the memory is a one time programmable memory.

5. The memory system of claim 1, the memory interface further comprising:

an output multiplex circuit connected to receive the second portion of the address, and to receive a block of output from each of the 2N columns and to supply therefrom (N+1) blocks of output in response to said second portion of the address.

6. The memory system of claim 1, wherein M is equal to eight.

7. The memory system of claim 6, wherein N is equal to 2^n, where n is a positive integer.

8. The memory system of claim 7, wherein n is equal to two.

9. A microprocessor, comprising:

a central processing unit with an instruction set including three-byte instructions;

a memory for storing the instructions, wherein the instructions are stored contiguously; and

a memory interface for supplying the instructions from the memory to the central processing unit, wherein each of said instructions is supplied in a single fetch operation.

10. The microprocessor of claim 9, wherein said instruction set further includes two-byte instructions and one-byte instructions.

11. The microprocessor of claim 9, wherein said memory is a one time programmable memory.

12. The microprocessor of claim 9, wherein said memory interface comprises a bus on which the instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

13. A method of operating a memory to supply up to (N+1) M-bit wide blocks of data simultaneously, where N and M are positive integers, comprising:

providing a memory logically organized as M bit wide blocks forming a plurality of rows of 2N columns;

providing an address specifying one of the memory block;

determining whether the address specifies a block in a first N of said columns;

supplying the address to the 2N columns if the address does not specify a block in the first N of said columns, and supplying the address to the first N of said columns and the portion of the address sufficient to specify the row to which the specified block belongs plus one to the second N of said columns if the address does specify a block in a first N of said columns; and

outputting the specified block and up to N adjacent blocks simultaneously.

14. The method of claim 13, further comprising:

disabling (N-1) of the columns in response to the column to which the specified block belongs.

15. The method of claim 14, further comprising:

programming said memory prior to said providing an address specifying one of the memory block.

16. The method of claim 13, wherein M is equal to eight.

17. The method of claim 16, wherein N is equal to 2^n, where n is a positive integer.

18. The method of claim 17, wherein n is equal to two.

19. A method of operating a memory to supply up to (N+1) M-bit wide blocks of data simultaneously, where N and M are positive integers, comprising:

providing a memory logically organized as M-bit wide blocks forming a plurality of rows of 2N columns;

providing an address specifying one of the memory block;

determining whether the address specifies a block in a first N of said columns;

supplying the up to (N+1) blocks of data simultaneously, wherein the blocks are from a plurality of rows if the specified block is in the first N of said columns and the blocks are from a single row if the specified block is not in the first N of said columns.

20. The method of claim 19, further comprising:

disabling (N-1) of the columns in response to the column to which the specified block belongs.

21. The method of claim 20, further comprising:

programming said memory prior to said providing an address specifying one of the memory block.

22. The method of claim 19, wherein M is equal to eight.

23. The method of claim 22, wherein N is equal to 2^n, where n is a positive integer.

24. The method of claim 23, wherein n is equal to two.

25. A method of operating a microprocessor, the microprocessor comprising a central processing unit with an instruction set including N-byte instructions, a memory for storing the instructions, and a memory interface for supplying the instructions from the memory to the central processing unit, wherein N is an integer greater than one, the method comprising:

logically organizing the memory as a plurality rows of M columns, wherein M is an integer greater than one and wherein N and M are relatively prime;

programming the instruction set into the memory, wherein the instructions are stored contiguously in the memory; and

operating the interface whereby each of the instructions can be supplied from the memory to the central processing unit in a single fetch operation.

26. The microprocessor of claim 25, wherein N is equal to three and M is equal to four.

27. The microprocessor of claim 26, wherein said instruction set further includes two byte instructions and one byte instructions.

28. The microprocessor of claim 26, wherein said memory interface comprises a bus on which the instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

29. The microprocessor of claim 25, wherein the memory is an embedded memory of the microprocessor.

30. The microprocessor of claim 29, wherein the memory is a one time programmable memory.